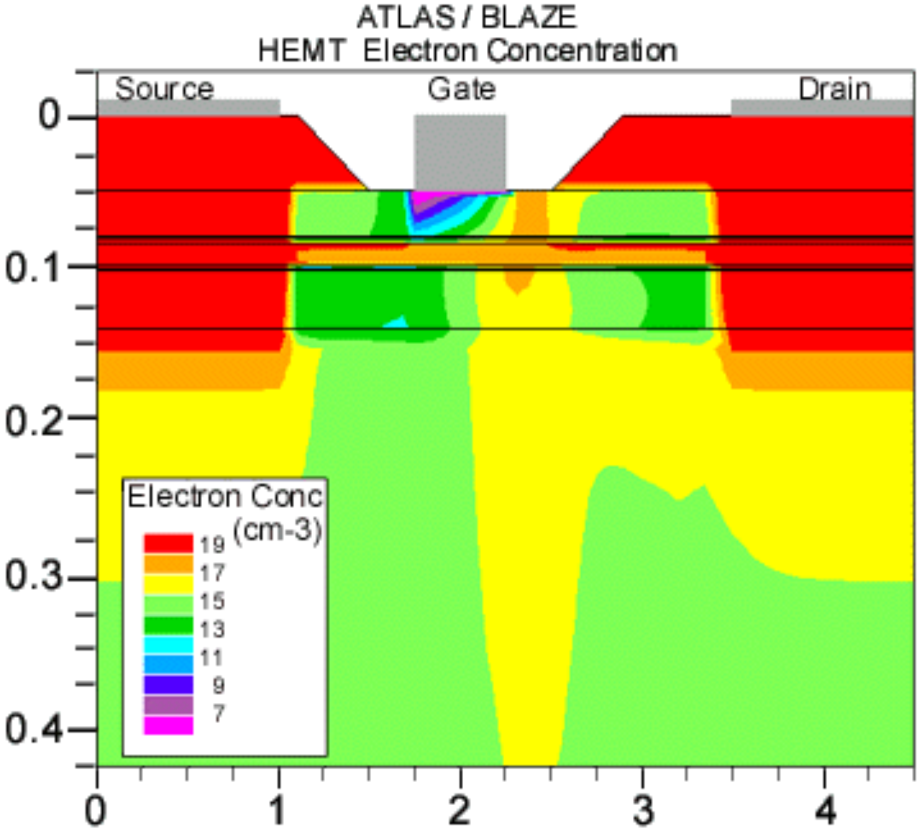
6.2, 5.8, 6.3 – JFET, MESFET, HEMTs

Image for this lecture… a tool used by device designers…

Silvaco ATLAS/BLAZE.

Numerical analysis, solve using a mesh of points to implement equations, and crunches the numbers over and over again to refine the final data-set. 2D or 3D. Can take days to complete one simulation!



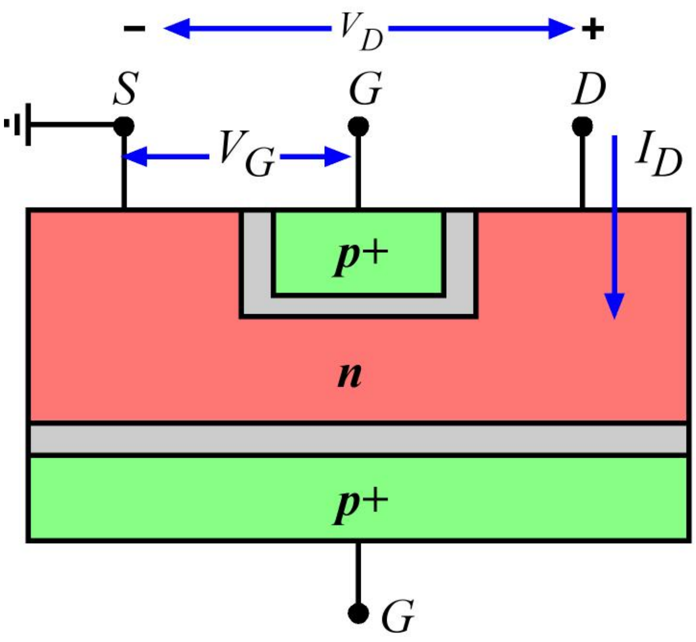
- Consider this 3 terminal device…

- Note the gate (G) electrodes are equivalent (shorted together)

- Apply V_D between drain (D) and source (S) and we get current flow

  … 'source' & 'drain' for electrons

- Apply negative voltage to G's… ☆



What happens that might be useful for a transistor?
Why the doping levels?

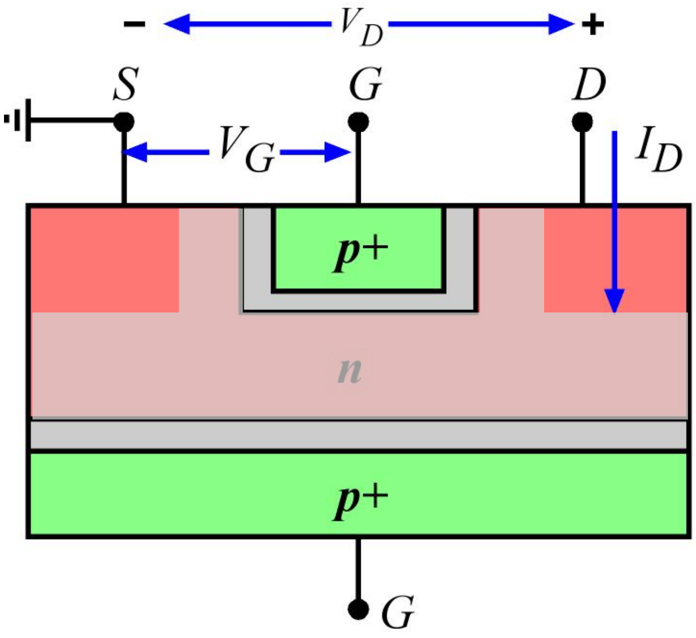
JFETs

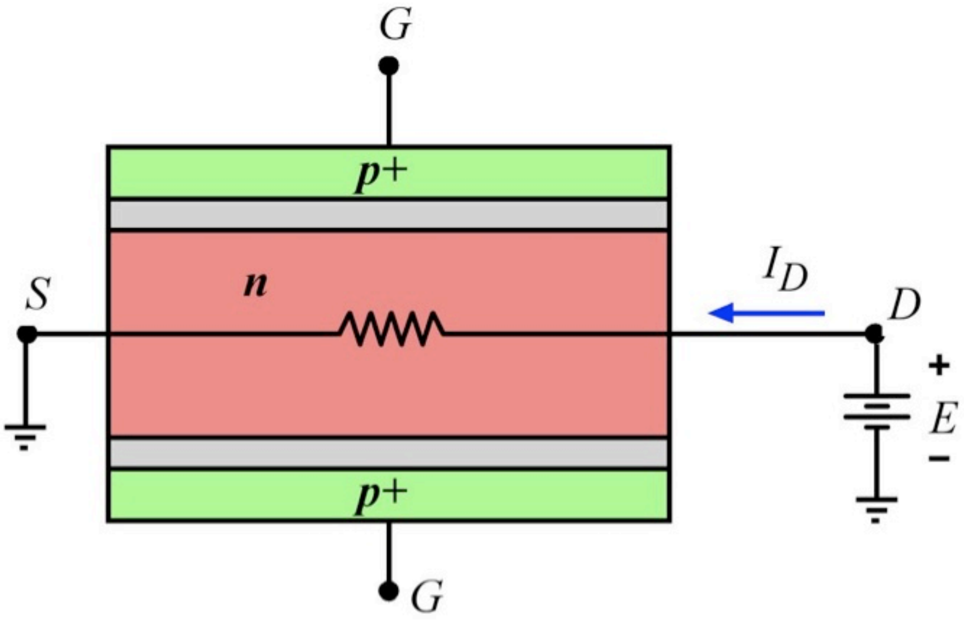
- Apply negative voltage to G's…

- Depletion regions expand, and can block the entire n-channel such that current flow is prohibited!

How much current did it take to reverse bias the PN junctions? ☆

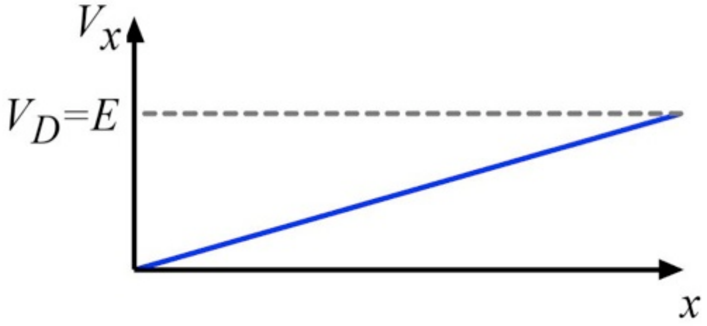
- Amplification using a Junction Field Effect Transistor (JFET)!





- We typically only need to focus on the channel region…

- What kind of current do we get? What carriers? I-V looks like what?

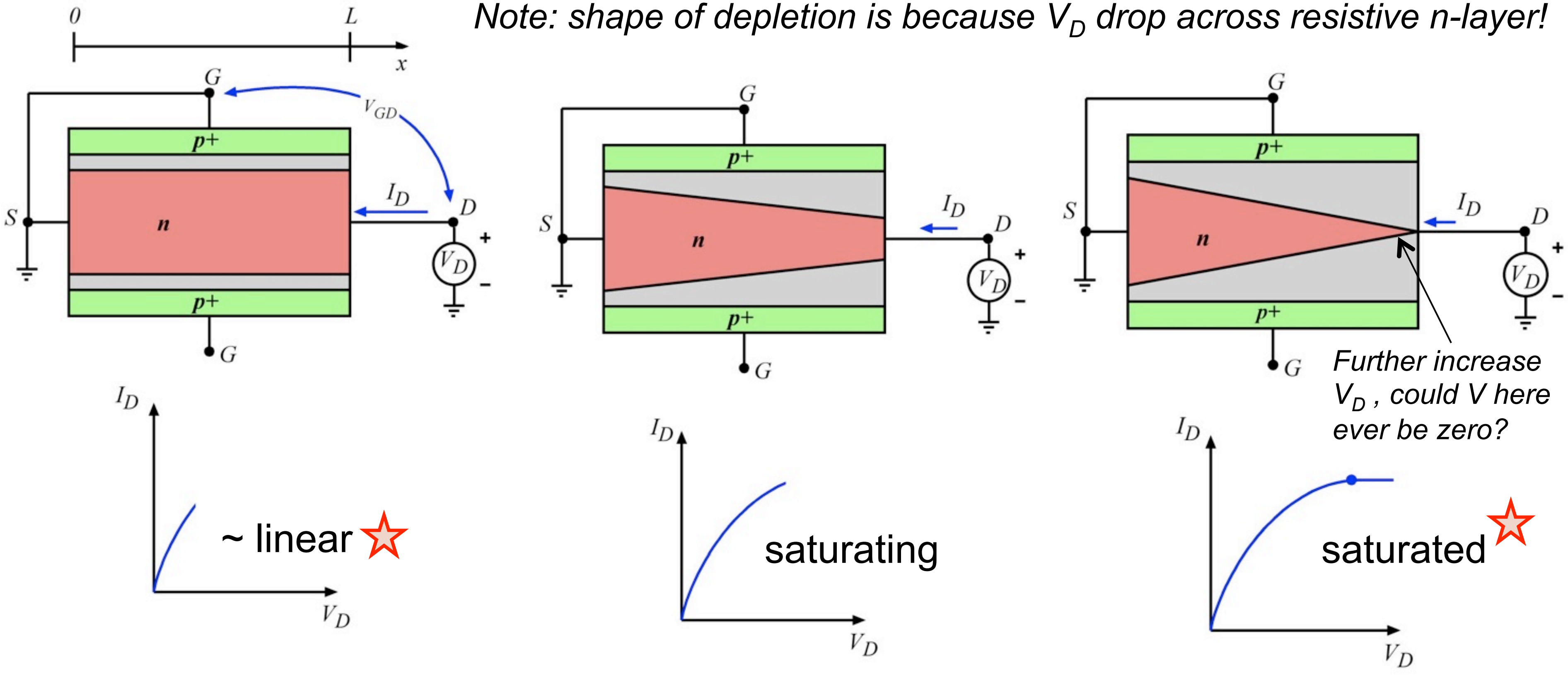


- However, a resistor behavior for the I-V is only valid for very low current levels…

- So what happens at higher current levels? Take a guess… hint, a resistor has a voltage drop across it…

JFETs

Note: shape of depletion is because V_D drop across resistive n-layer!



~ linear ☆

saturating

saturated ☆

Further increase V_D , could V here ever be zero?

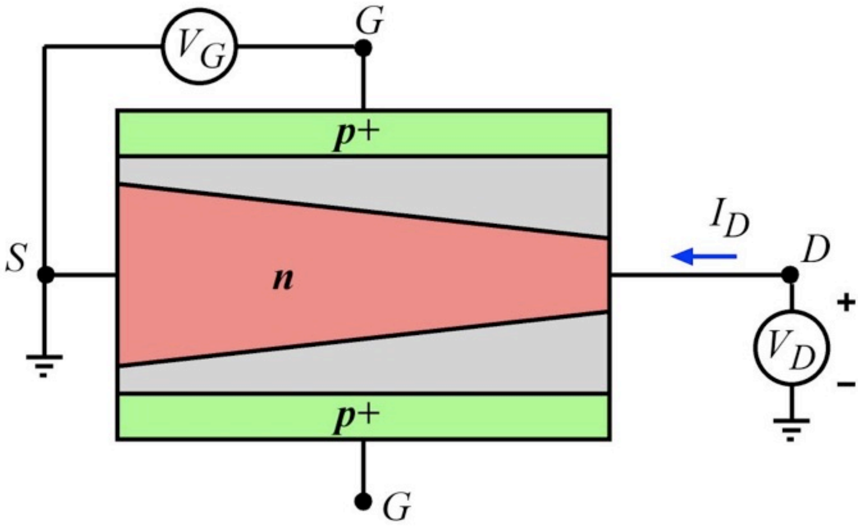
- At higher current levels we can get Pinch-off (for Vg=Vs=0).

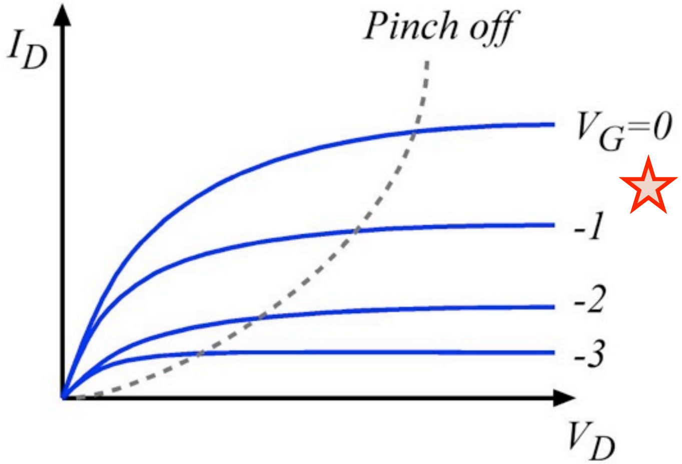
Increase drain voltage V_D, the V_{DS} increases which should increase current flow.

However, increasing V_D reverse biases the PN junctions and 'pinches-off' the channel (causes current <u>saturation</u>). Depletion width tapered due to <u>voltage drop</u>…

- We can bias V_G and modulate the n-channel conductivity (depletion)
- Therefore we have created a transistor…
- Note, if we operated in saturation, small changes in V_G will cause large changes in I_D. And I_G is small!
- Reverse dopings, how would Vg change?
- Check out this great simulation… try it out! Use the link or Google 'JFET CAM UK'

  http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/jfet.html





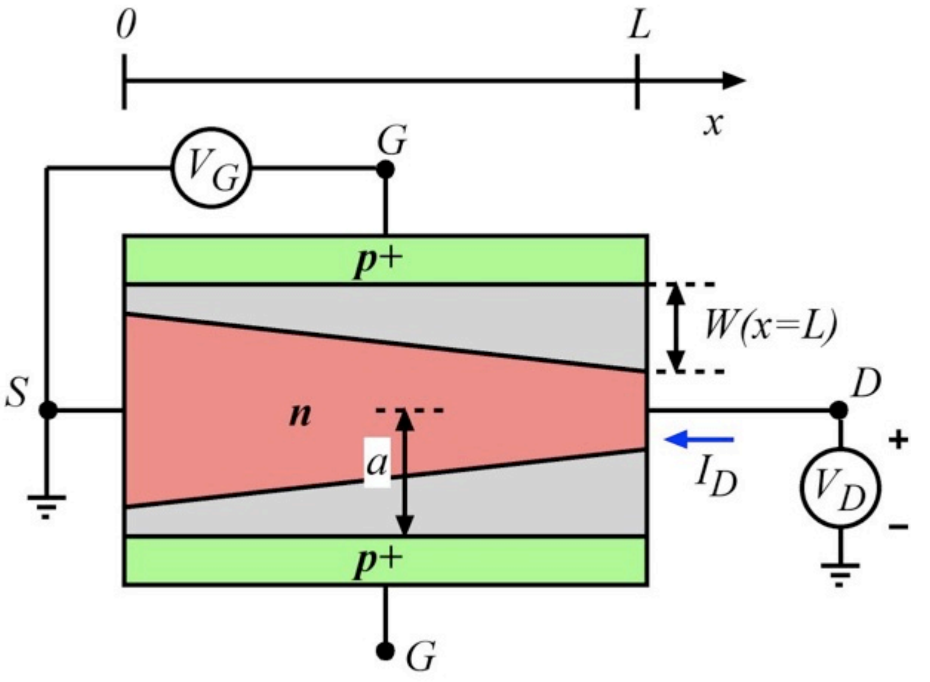
JFETs

- Recall depletion region thickness for a pn junction.

$$V_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

$$W = \sqrt{\frac{2\varepsilon kT}{q^2}\left(\ln\frac{N_A N_D}{n_i^2}\right)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$

$$W = \sqrt{\frac{2\varepsilon V_0}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$



- At a reverse bias V…

$$W = \sqrt{\frac{2\varepsilon(V_0 - V)}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$

- The junction is p+ so $N_A >> N_D$, we can use this and $V_0 << V_{GD}$ to approximate W as…

$$W \approx \sqrt{\frac{2\varepsilon(-V_{GD})}{qN_D}}$$

…at pinch off W=a

Introduce Vp (*W*=*a*) and solve for it…

$$-V_{GD}(pinchoff) = V_P$$

$$V_p = \frac{q a^2 N_D}{2\varepsilon}$$

Why dep. on N_d only?

- Recall effect of resistivity (ρ):

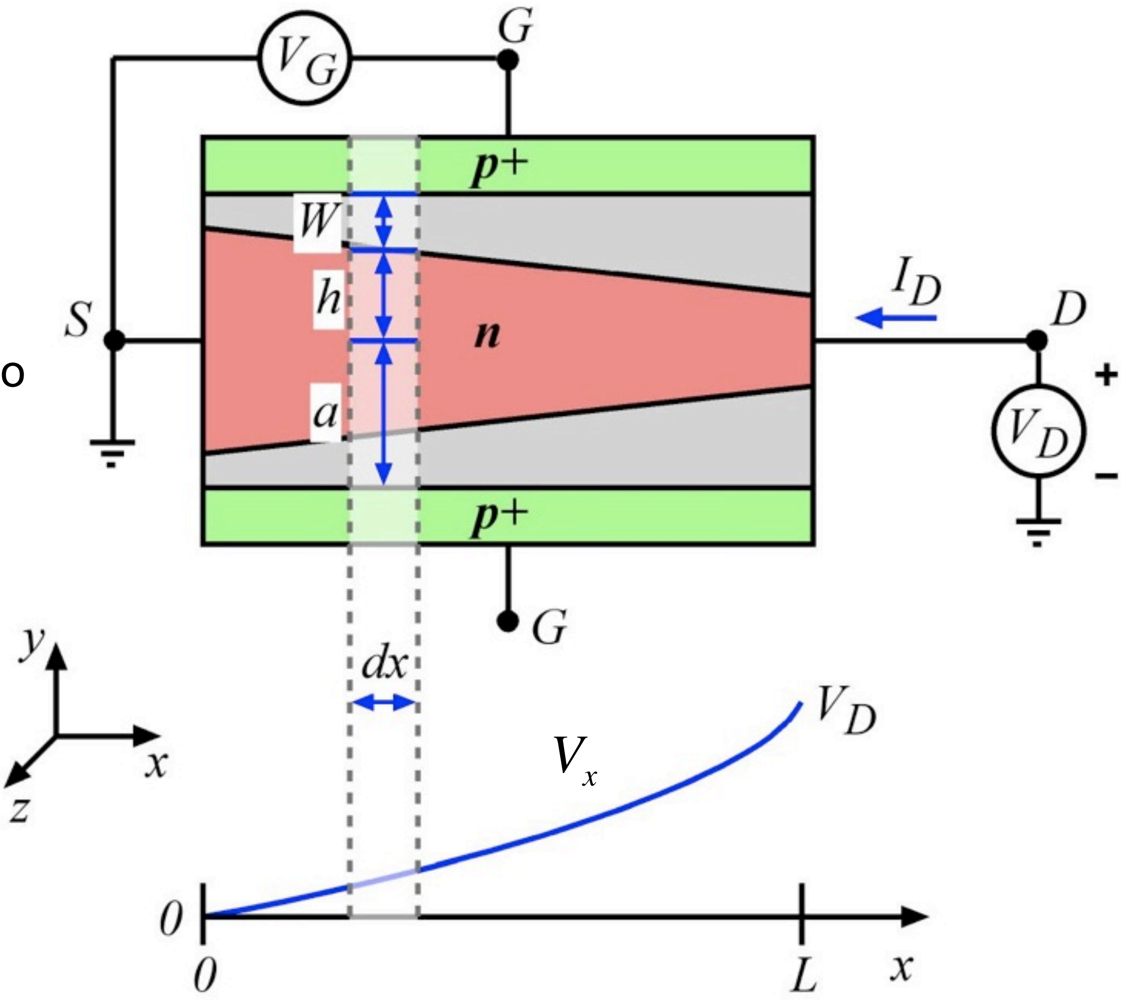
$$R = \frac{\rho(\Omega - cm)L}{A} = \frac{\rho L}{wt}$$

- For the system at right substitute new values for L->dx and t->2h(x) to obtain the *differential* resistance:

$$R = \frac{\rho\, dx}{Z\, 2h(x)}$$

- Therefore current is (a differential equation, 1st order, easiest to solve!):

$$I_D = V/R = \frac{Z\, 2h(x)}{\rho}\frac{dV_x}{dx}$$



'gradual channel approximation', no abrupt change in h(x) with dx

- We already know that:

$$V_p = \frac{q a^2 N_D}{2\varepsilon} \qquad V_{Gx} = V_G - V_x$$

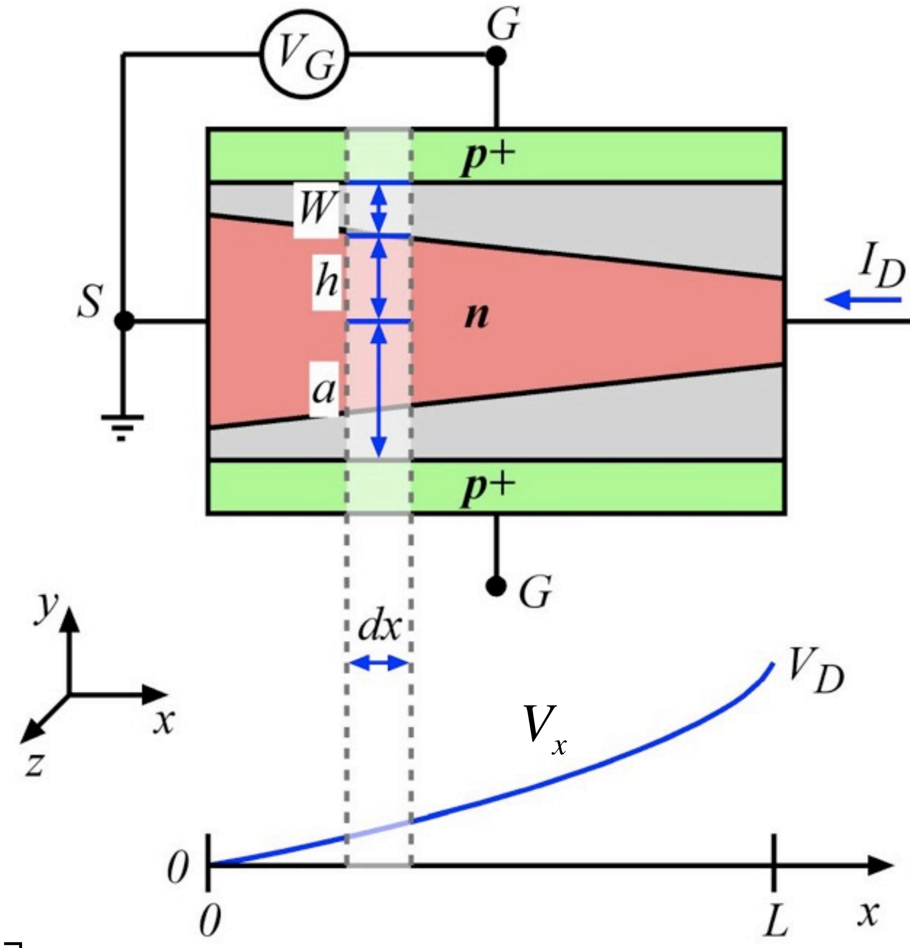
$$W(x) \approx \sqrt{\frac{2\varepsilon(-V_{Gx})}{qN_D}}$$

- The half width of the channel h(x)

$$h(x) = a - W(x)$$

using above terms we can show that…

$$\Rightarrow \quad h(x) = a\left[1 - \sqrt{\frac{V_x - V_G}{V_P}}\right]$$

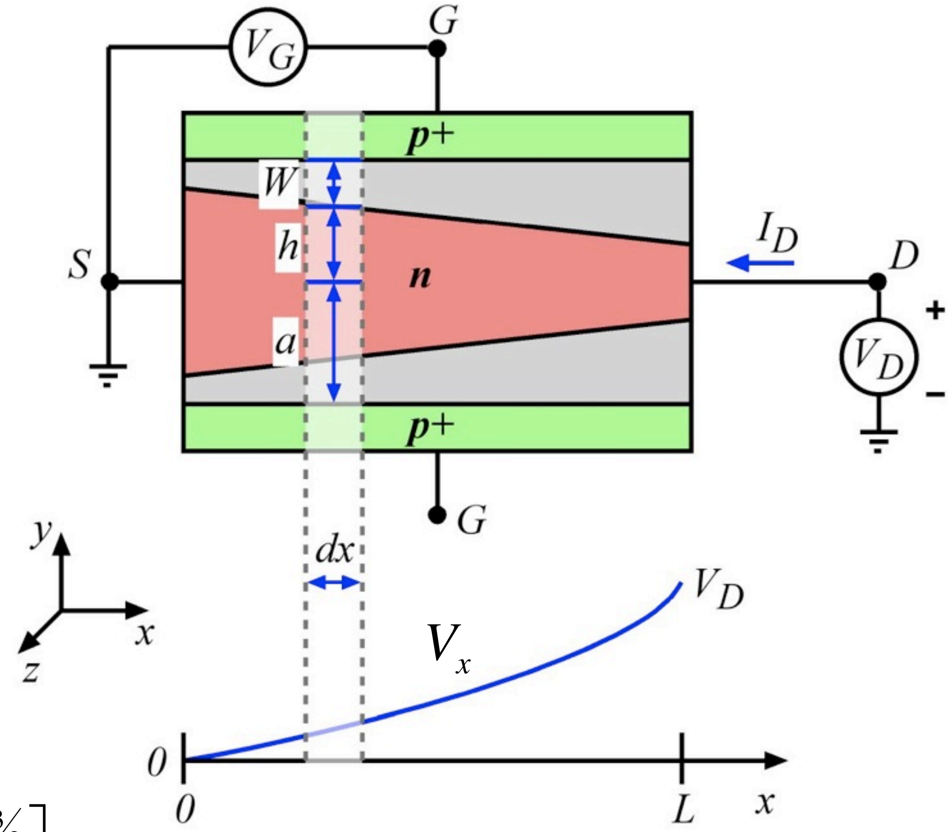


- Substitute: $h(x) = a\left[1 - \sqrt{\dfrac{V_x - V_G}{V_P}}\right]$
- Into: $I_D = V/R = \dfrac{Z\,2h(x)}{\rho}\dfrac{dV_x}{dx}$
- Leads to:

$$I_D dx = \frac{2Za}{\rho}\left[1 - \sqrt{\frac{V_x - V_G}{V_P}}\right]dV_x$$

integrate both sides
(but over what limits?)

$$I_D L = \frac{2Za}{\rho}V_P\left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\left(\frac{V_D - V_G}{V_P}\right)^{3/2}\right]$$



$$G_0 = \frac{2aZ}{\rho L}$$ *conductance for the channel (mho's)*

for low current levels

$$I_D = G_0 V_P\left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\left(\frac{V_D - V_G}{V_P}\right)^{3/2}\right]$$

JFETs

- Keep increasing Vd, at higher current levels we run into pinch-off and this term goes to unity (why?)

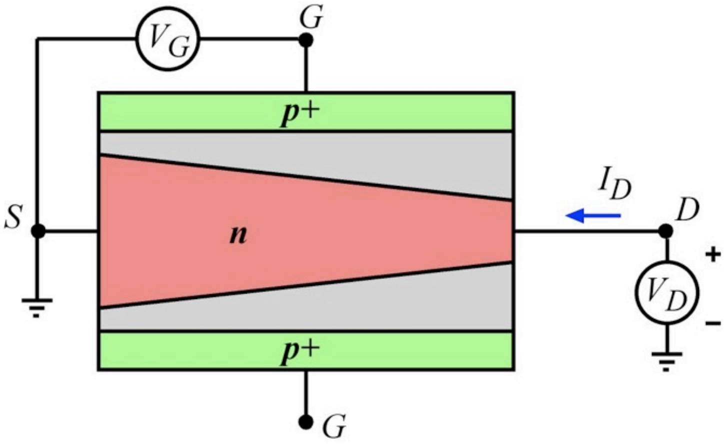
$$V_D - V_G = V_P$$

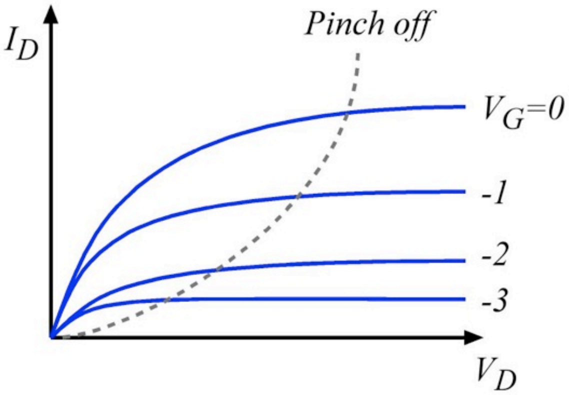
$$I_D = G_0 V_P\left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\left(\cancel{\frac{V_D - V_G}{V_P}}\right)^{3/2}\right]$$

$$I_D(sat.) = G_0 V_P\left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\right]$$

$$V_P = V_D - V_G \Rightarrow \quad \frac{V_D}{V_P} = 1 + \frac{V_G}{V_P}$$

Lets get rid of Vd…. first divide both sides by Vp and reorder.





So why for Id(sat.) is there no V_D term? ☆

$$I_D(sat.) = G_0 V_P\left[\frac{V_G}{V_P} - \frac{2}{3}\left(\frac{V_G}{V_P}\right)^{3/2} + \frac{1}{3}\right]$$

JFETs

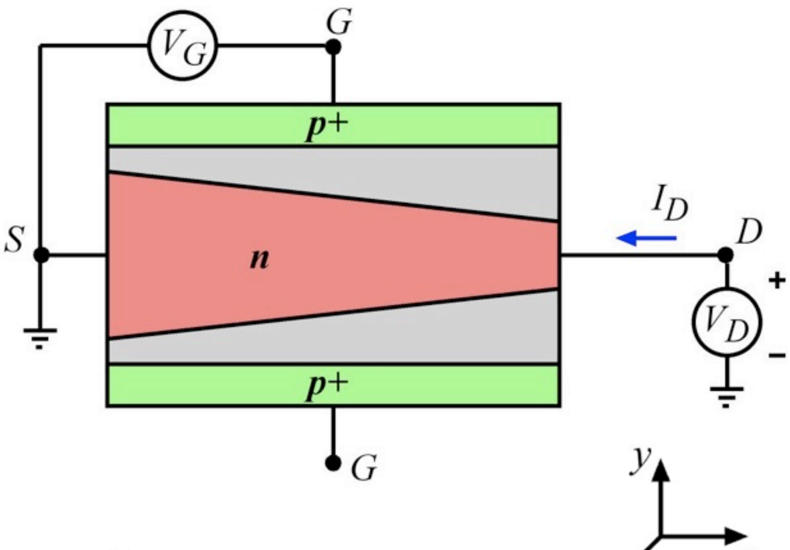
- We can represent the device *in the saturation region* with an equivalent circuit:

$$I_D(sat.) = G_0 V_P \left[\frac{V_G}{V_P} - \frac{2}{3}\left(\frac{V_G}{V_P}\right)^{3/2} + \frac{1}{3} \right]$$

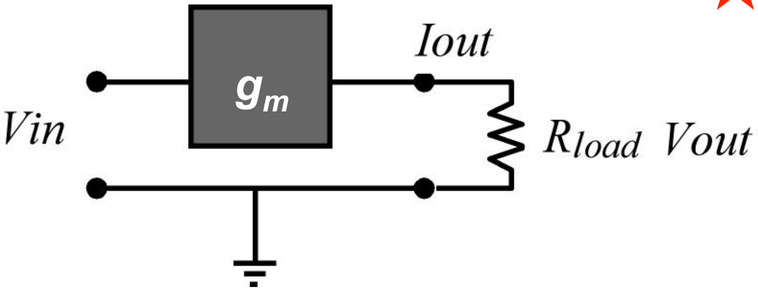
channel conductance

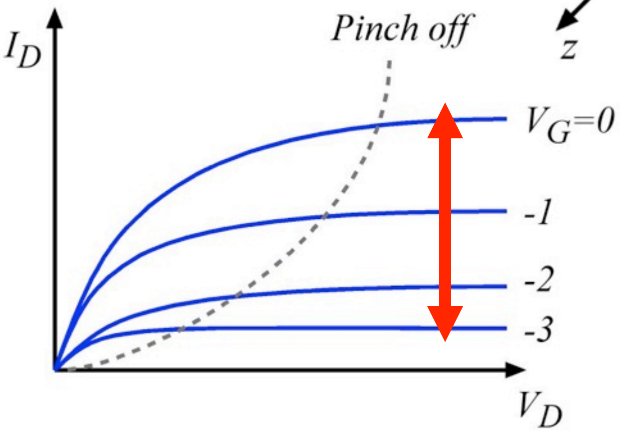
$$G_0 = \frac{2aZ}{\rho L}$$

$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} = G_0\left[1 - \left(\frac{-V_G}{V_P}\right)^{1/2}\right] \quad ,(V_G < 0)$$



- g_m has units of A/V (S or mhos). But it is more than just conductance, it transfers an input voltage to an output current… *Transconductance!*





- If you pick an apple from a tree, and find it has transconductance, you could represent it this way! (It doesn't though, FYI… :)

- JFET F.O.M. is g_m/Z

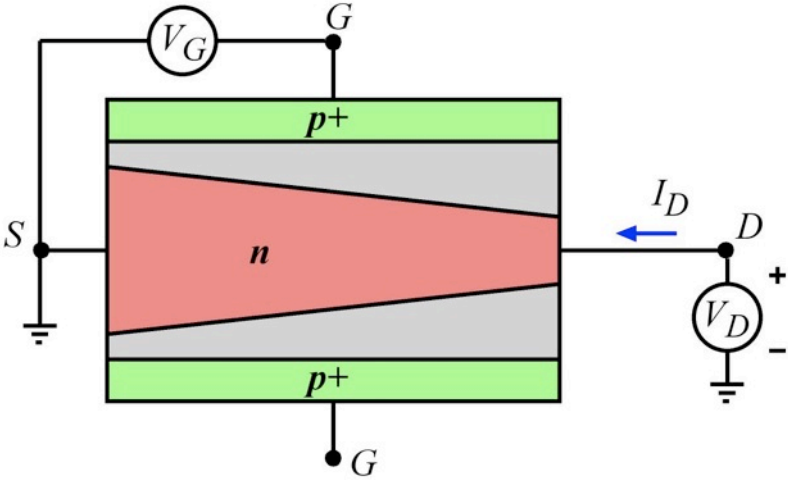
large amplification or switching with min device area…

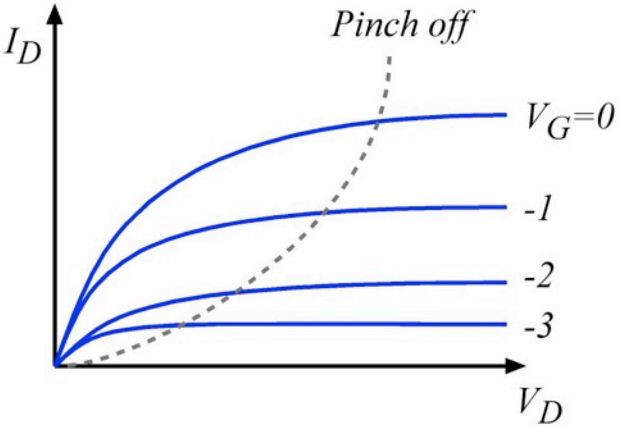
- Lastly, It can be shown experimentally that:

$$I_D(sat.) \cong I_{DSS}\left(1+\frac{V_G}{V_P}\right)^2 \qquad (V_G<0)$$

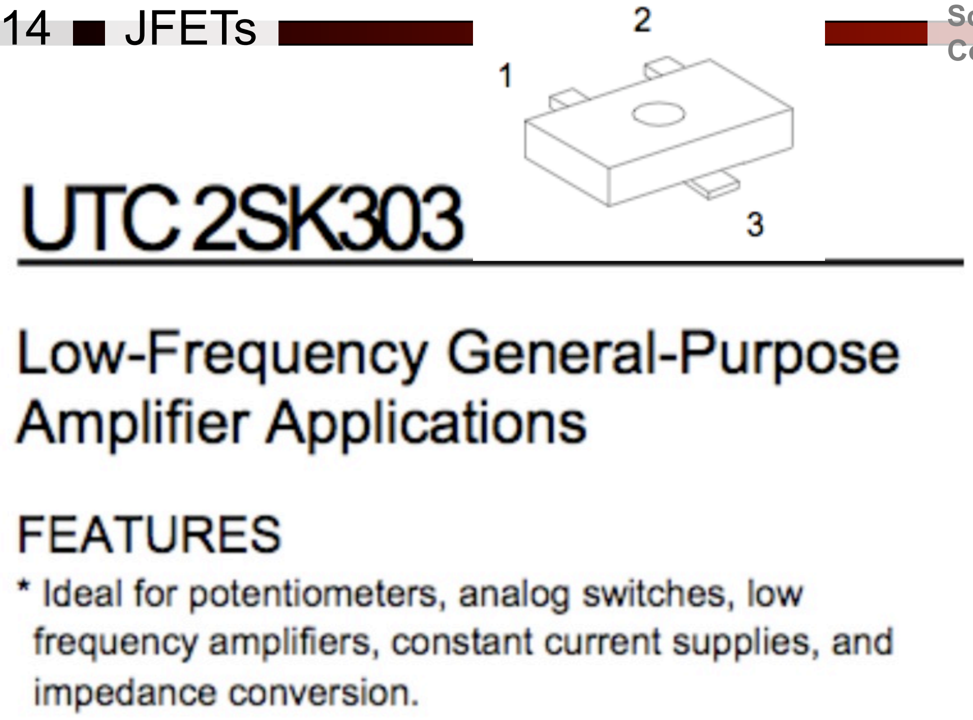
- Where I_{DSS} is the saturated drain current with $V_G=0$

$$I_{DSS} = {}^1\!/_3\, G_0 V_P = \frac{2aZ}{3\rho L} V_P$$





JFETs

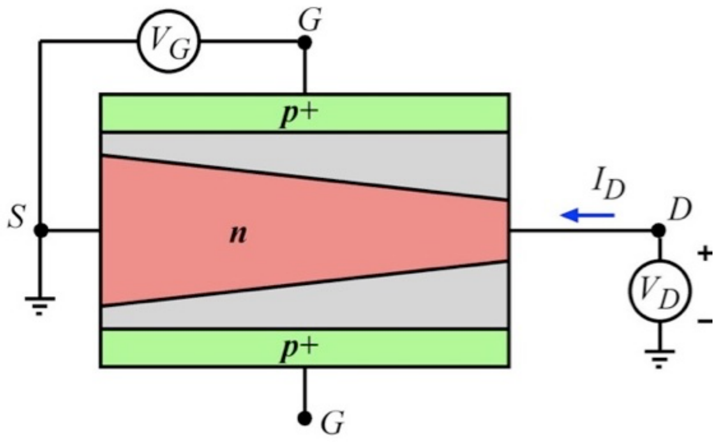


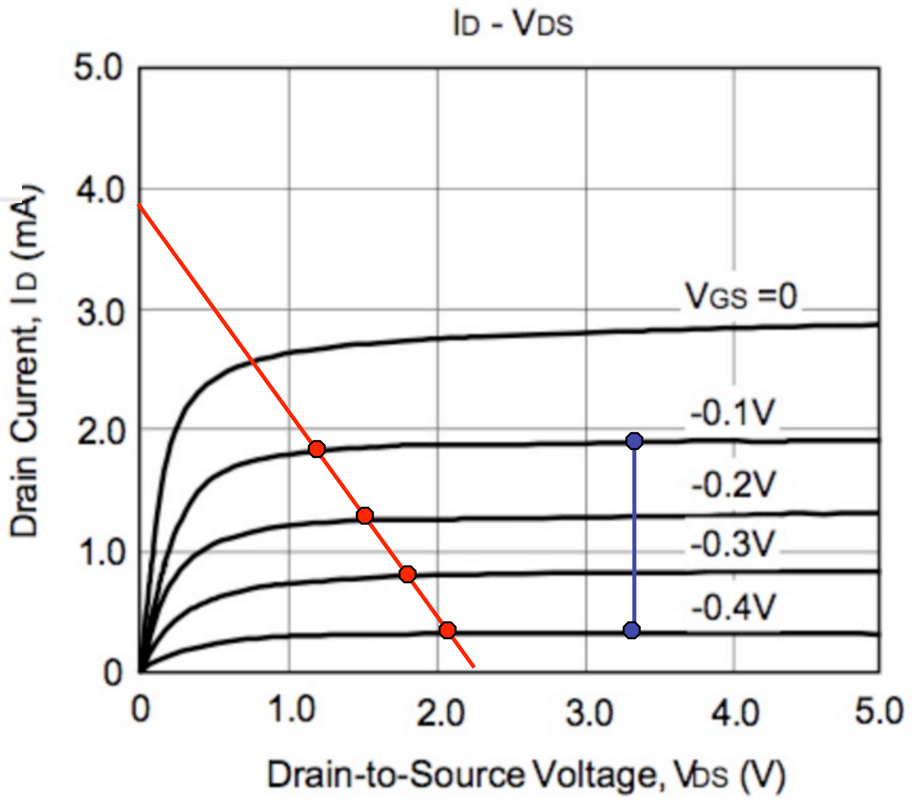
UTC 2SK303

Low-Frequency General-Purpose Amplifier Applications

FEATURES

* Ideal for potentiometers, analog switches, low frequency amplifiers, constant current supplies, and impedance conversion.

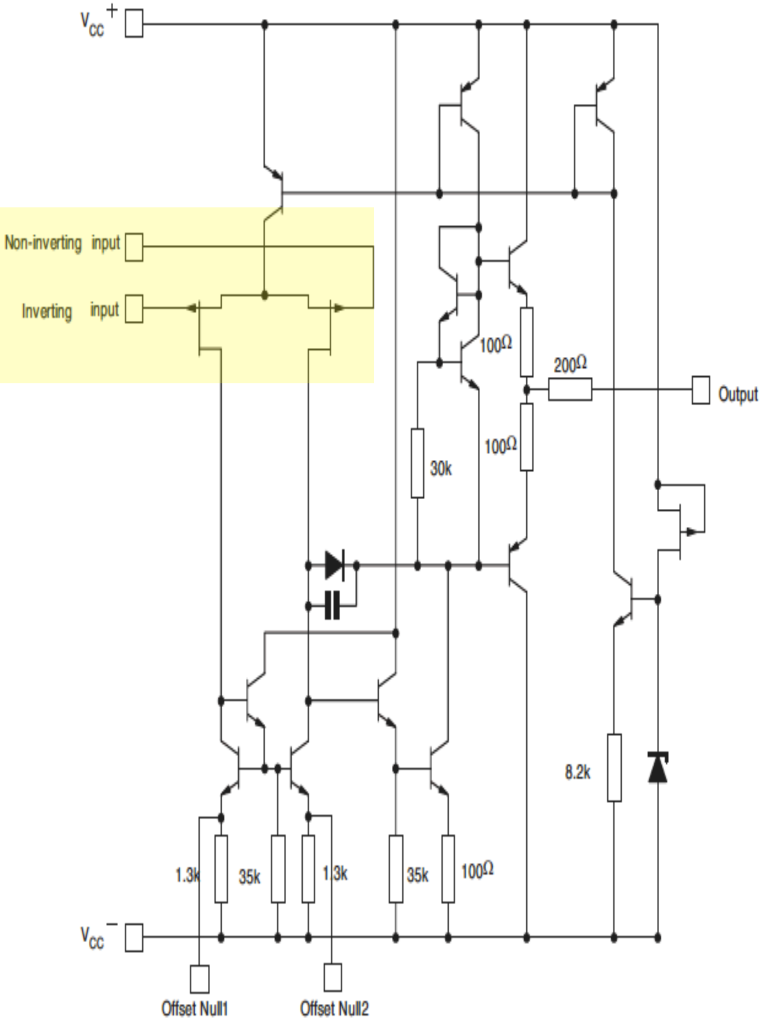


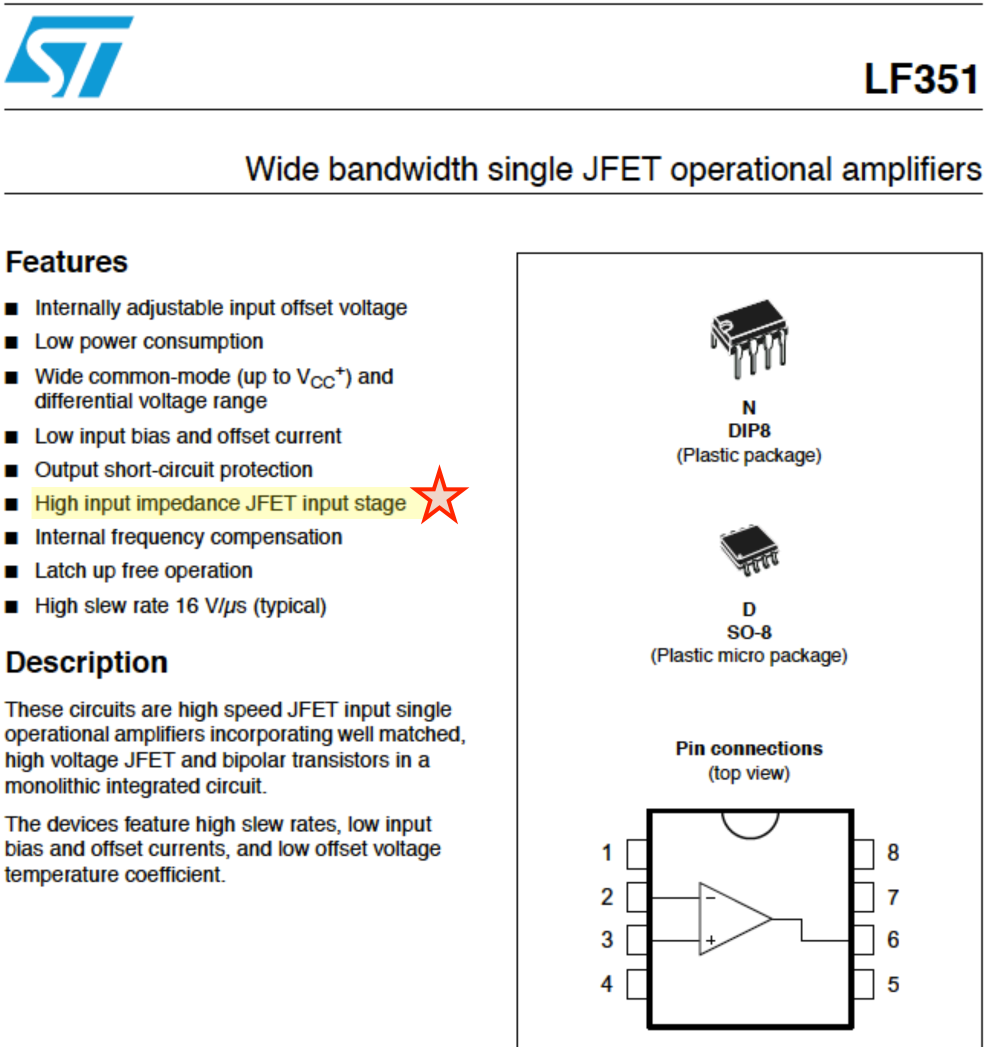


JFETs used when need high current output with very low current input at gate (some BJT's have too much input current, some MOSFET not enough output current).

$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} = \frac{(1.8-0.3)mA}{0.3\,V}$$

easy to calculate g_m ~5×10^{-3} mhos





LF351

Wide bandwidth single JFET operational amplifiers

Features

- Internally adjustable input offset voltage
- Low power consumption
- Wide common-mode (up to V_{CC}^+) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage ☆
- Internal frequency compensation
- Latch up free operation
- High slew rate 16 V/μs (typical)

Description

These circuits are high speed JFET input single operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

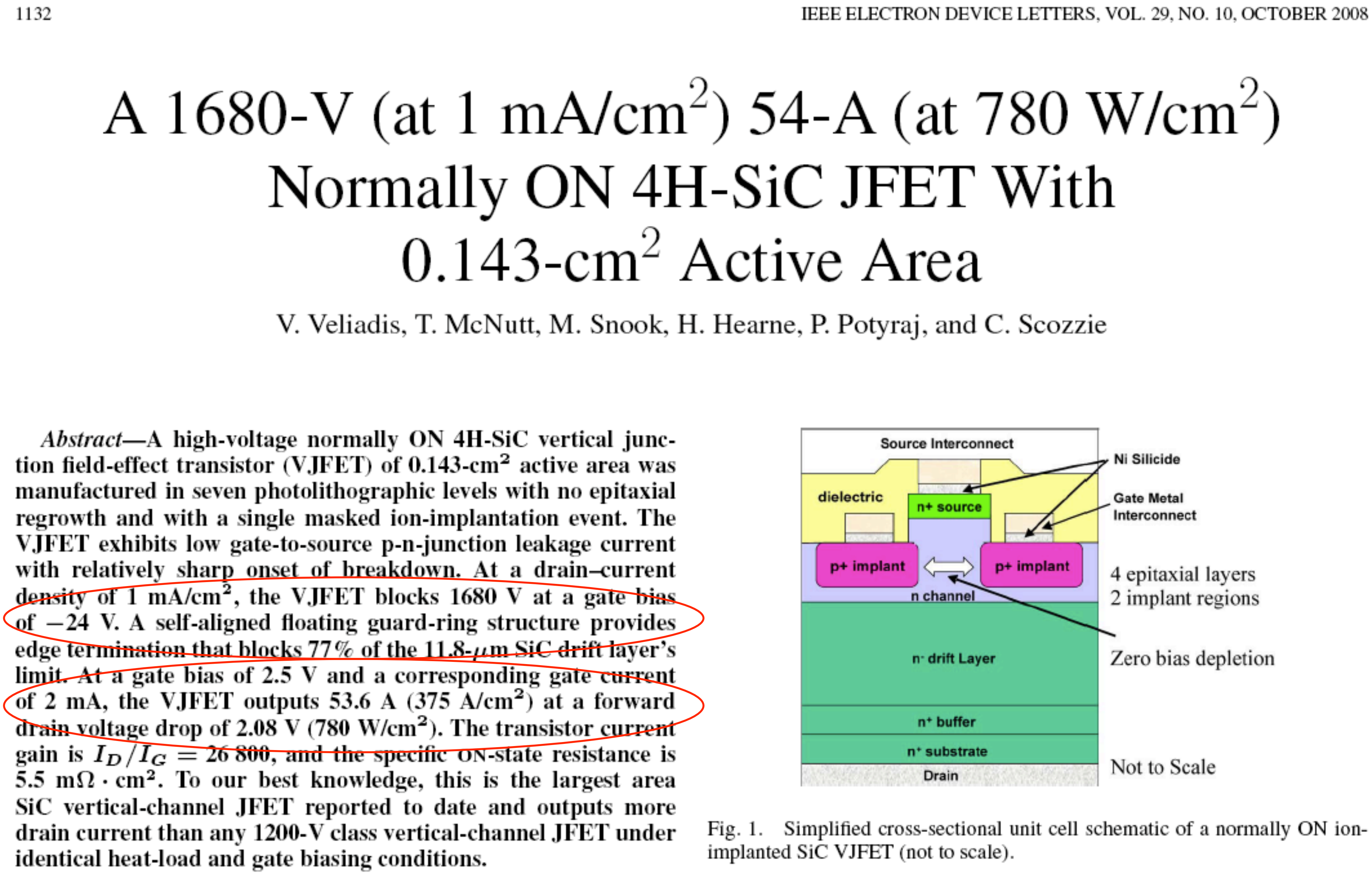
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

N
DIP8
(Plastic package)

D
SO-8
(Plastic micro package)

Pin connections
(top view)

Wow! >50! Vertical JFET?



1132 IEEE ELECTRON DEVICE LETTERS, VOL. 29, NO. 10, OCTOBER 2008

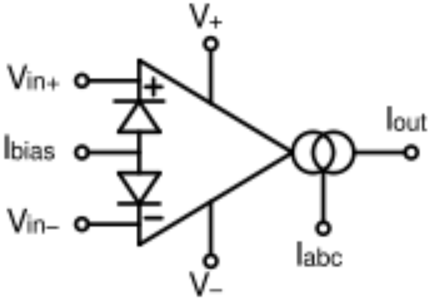
A 1680-V (at 1 mA/cm^2) 54-A (at 780 W/cm^2) Normally ON 4H-SiC JFET With 0.143-cm^2 Active Area

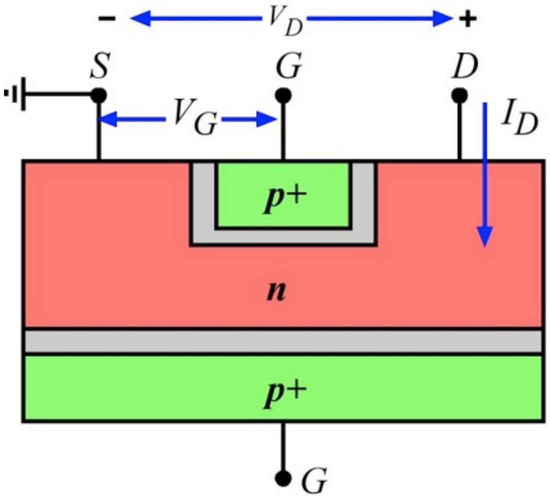
V. Veliadis, T. McNutt, M. Snook, H. Hearne, P. Potyraj, and C. Scozzie

Abstract—A high-voltage normally ON 4H-SiC vertical junction field-effect transistor (VJFET) of 0.143-cm^2 active area was manufactured in seven photolithographic levels with no epitaxial regrowth and with a single masked ion-implantation event. The VJFET exhibits low gate-to-source p-n-junction leakage current with relatively sharp onset of breakdown. At a drain–current density of 1 mA/cm^2, the VJFET blocks 1680 V at a gate bias of -24 V. A self-aligned floating guard-ring structure provides edge termination that blocks 77% of the 11.8-μm SiC drift layer's limit. At a gate bias of 2.5 V and a corresponding gate current of 2 mA, the VJFET outputs 53.6 A (375 A/cm^2) at a forward drain voltage drop of 2.08 V (780 W/cm^2). The transistor current gain is $I_D/I_G = 26\,800$, and the specific ON-state resistance is 5.5 m$\Omega \cdot$ cm^2. To our best knowledge, this is the largest area SiC vertical-channel JFET reported to date and outputs more drain current than any 1200-V class vertical-channel JFET under identical heat-load and gating biasing conditions.

Fig. 1. Simplified cross-sectional unit cell schematic of a normally ON ion-implanted SiC VJFET (not to scale).

- Warmup, why is this called an operational *transconductance* amplifier?





- Do I need positive or negative gate voltage to turn off the JFET?

- If we keep increasing JFET drain voltage, what happens? *Does the current keep increasing more and more, if not, what is this called? There are two terms describing this, one term is for the voltage at which this occurs, and the other term describes the current.*

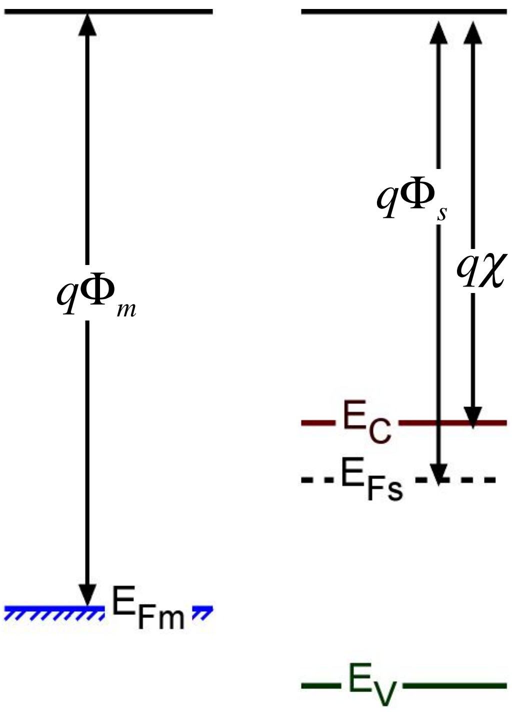
- Why is the JFET gate heavily doped? *Hint, thing of the direction you want depletion to go…*

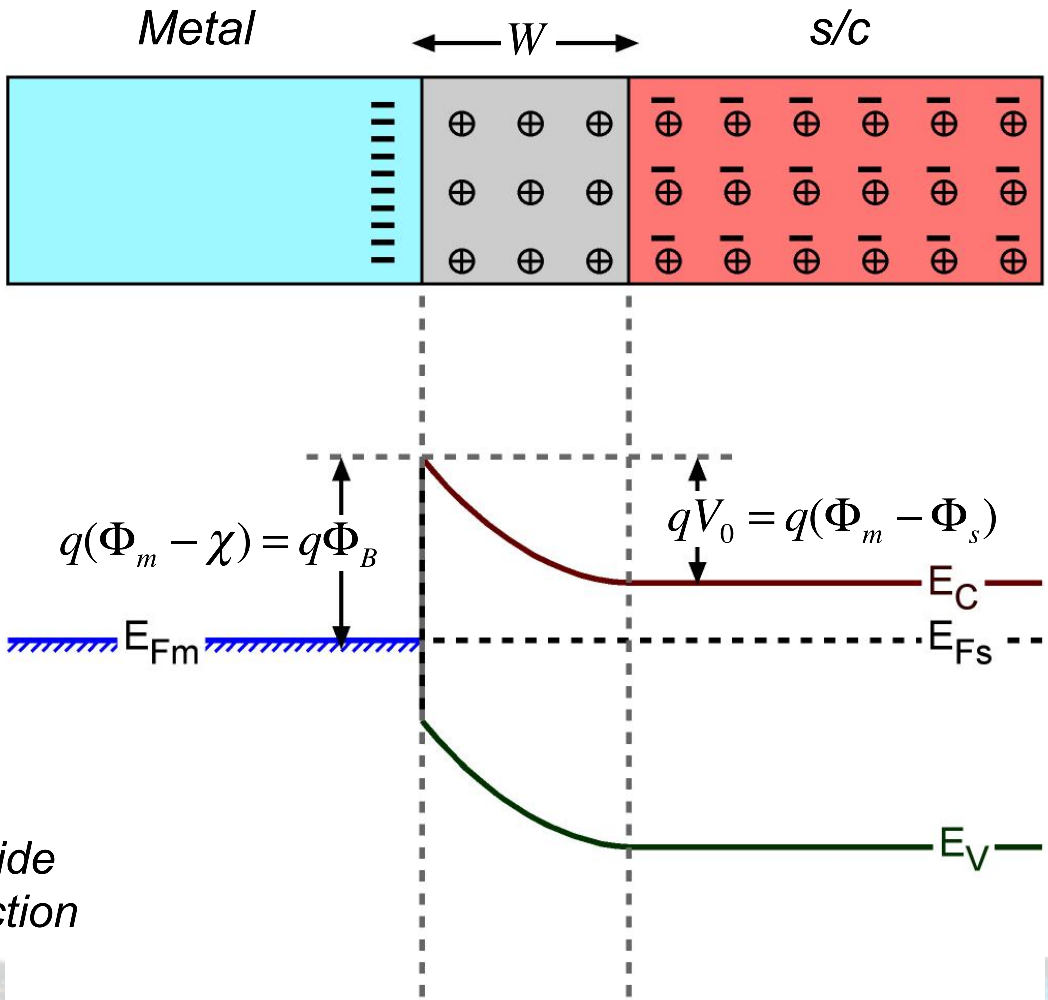
- Why is a key advantage of using a JFET? *Hint, the best amplifiers have very high input impedance (don't require alot of input voltage or current).*

(a) zero input current, and high output current;
(b) very small input current, and high output current;
(c) large input current, and low output current;
(d) small input current, and small output current;

Switch Gears… Don't need PN!

- Remember, metal has a such a high density of electrons that it acts like n++.

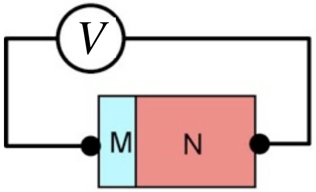


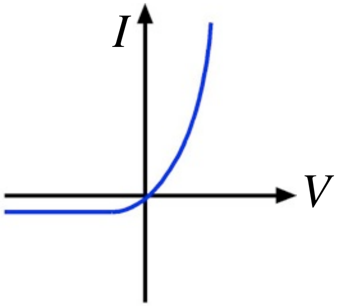


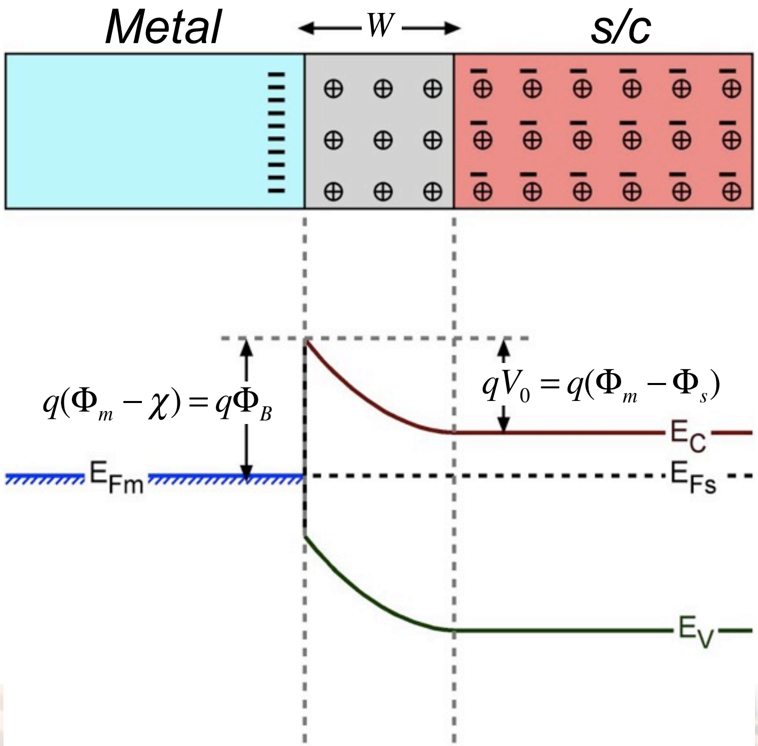
…remember semiconductor side looks just like 1/2 of a PN junction

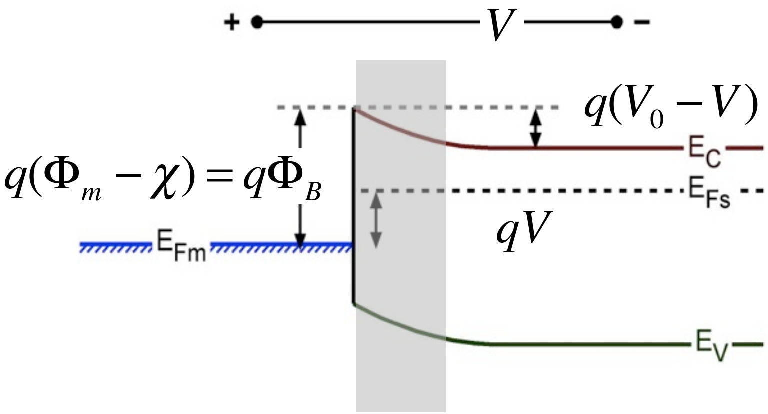
Key is Depletions Width…

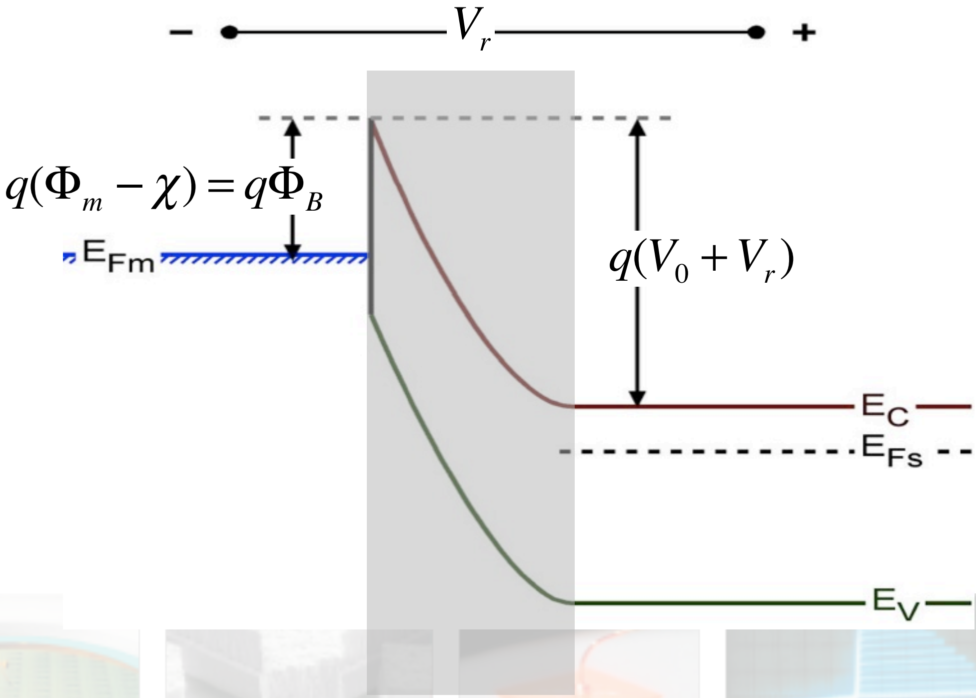
- N-type Schottky Diode with $\Phi_m > \Phi_s$







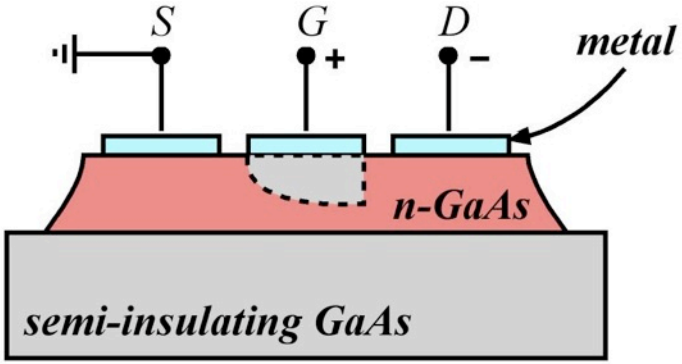


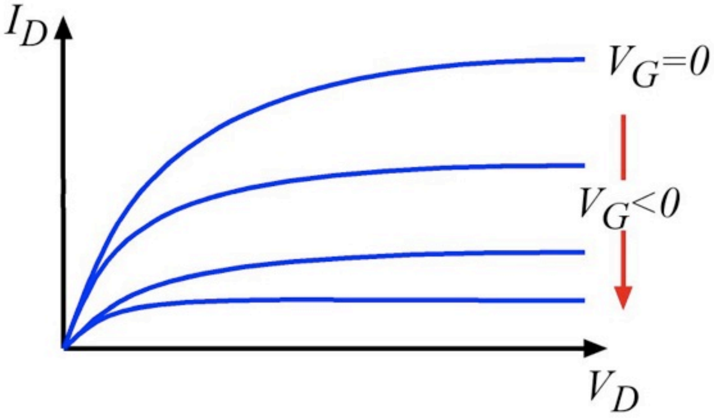


Key is Depletions Width…

- MESFET
  -only metal contacts
- Depletion modulation using a Schottky Diode
- n-GaAs epitaxy grown on insulating GaAs subs.
- Etched to <u>isolate</u> devices (C, and J leakage!)
- Only need for high resolution patterning is the metal electrodes…
- So why make a GaAs MESFET instead of a Si MOSFET or JFET? Looking for 3 answers…

Au-Ge : ohmic
Al : Schottky



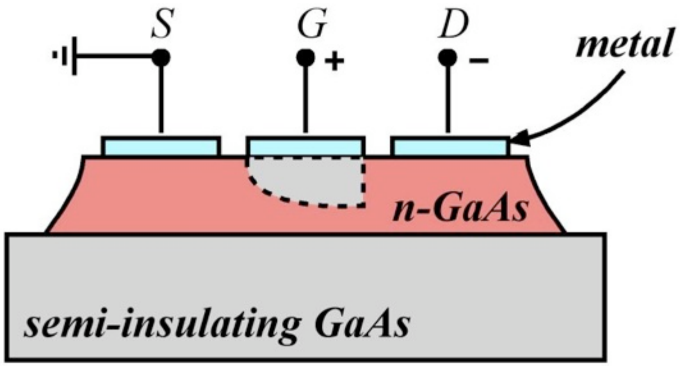


(1) wider Eg (1.12➔1.43 eV) for higher current
(2) higher e mobility (1350➔8500 cm^2/V-s)
(3) small features (only pattern metal!)

…. we will go through these in detail on the next slide.

MESFET

- Why higher speed?



1) for a fixed n, E, we get higher J as μ increases. We get higher speed! More charges get across per unit time to charge up the next line in the circuit!

$$J_{drift} = q\mu_n n_n \mathrm{E}$$

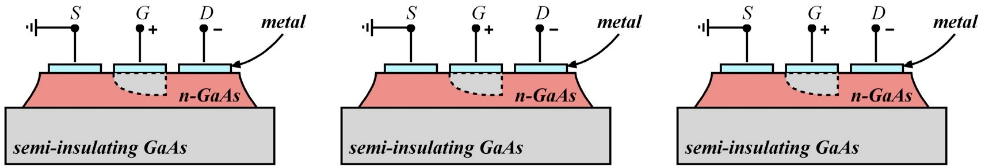
$$\mu_n = 8500\ \mathrm{cm^2/V\text{-}s}$$

2) Wider bandgap (1.43 eV)

Wider bandgap allows higher temperature… why? What does this mean in terms of device size & speed?

3) Very simple fabrication allows smaller features, how does this help us?

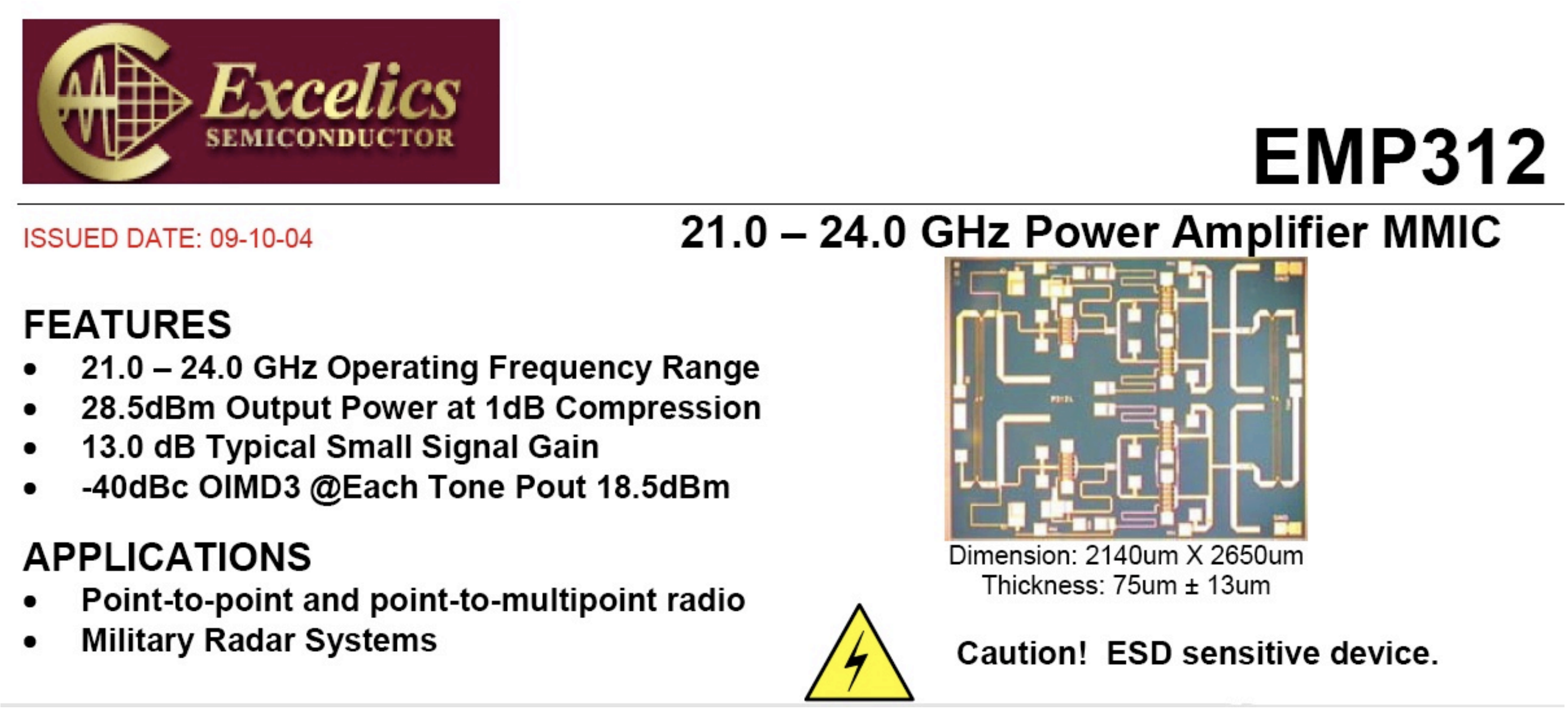
Think about connecting the source of one JFET to the gate of another JFET, why would a smaller gate help us???



RC IS EVERYTHING FOR HIGH SPEED! Narrow gate = lower R, Narrow gate = smaller C! Smaller gates for all FET devices!!!!

MESFET MMIC

Monolithic Microwave IC - an analog IC with on-chip capacitors and inductors design to work at microwave frequencies.



Excelics SEMICONDUCTOR

EMP312

ISSUED DATE: 09-10-04

21.0 – 24.0 GHz Power Amplifier MMIC

FEATURES

- 21.0 – 24.0 GHz Operating Frequency Range
- 28.5dBm Output Power at 1dB Compression
- 13.0 dB Typical Small Signal Gain
- -40dBc OIMD3 @Each Tone Pout 18.5dBm

APPLICATIONS

- Point-to-point and point-to-multipoint radio
- Military Radar Systems

Dimension: 2140um X 2650um
Thickness: 75um ± 13um

Caution! ESD sensitive device.

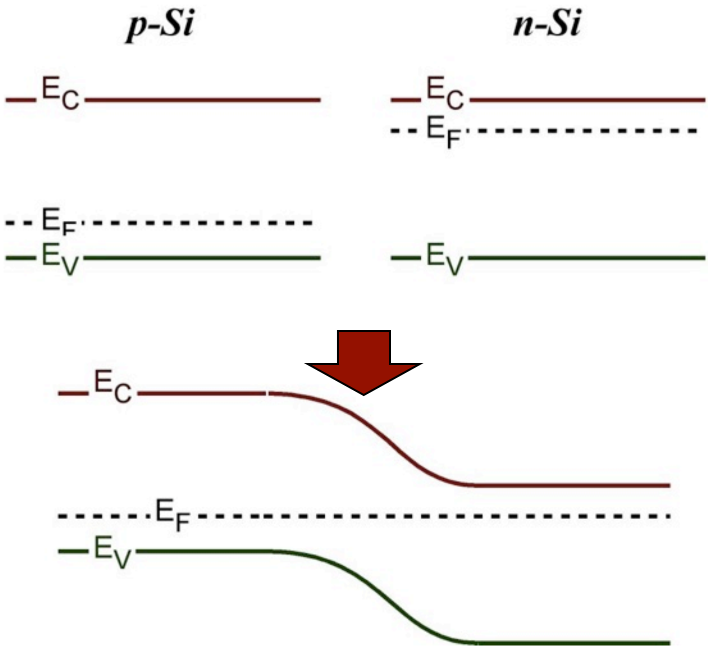
I_{dss} = 1 A! Power dissipation up to 12 W, *cooling?*

Back to Heterojunctions…

- Homojunction implies same material, bandgap and electron affinities (χ) are the same so conduction and valence bands line up, only work function (Φ) is different…

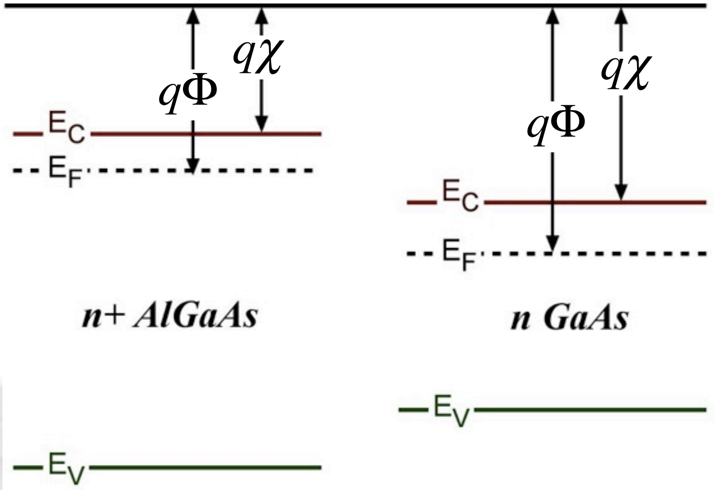
- Homojunctions are easy to make (diffusion).

- However, the highest performance LEDs/lasers, BJTs, and a device called a HEMT all need heterojunctions (and for HEMT, the benefit is quantum confinement).



- Consider two different materials such as GaAs (~1.42) and AlGaAs (~1.8 eV) with different work function (Φ), ***bandgaps, and electron affinities (χ).***

- What must happen?



Heterojunctions

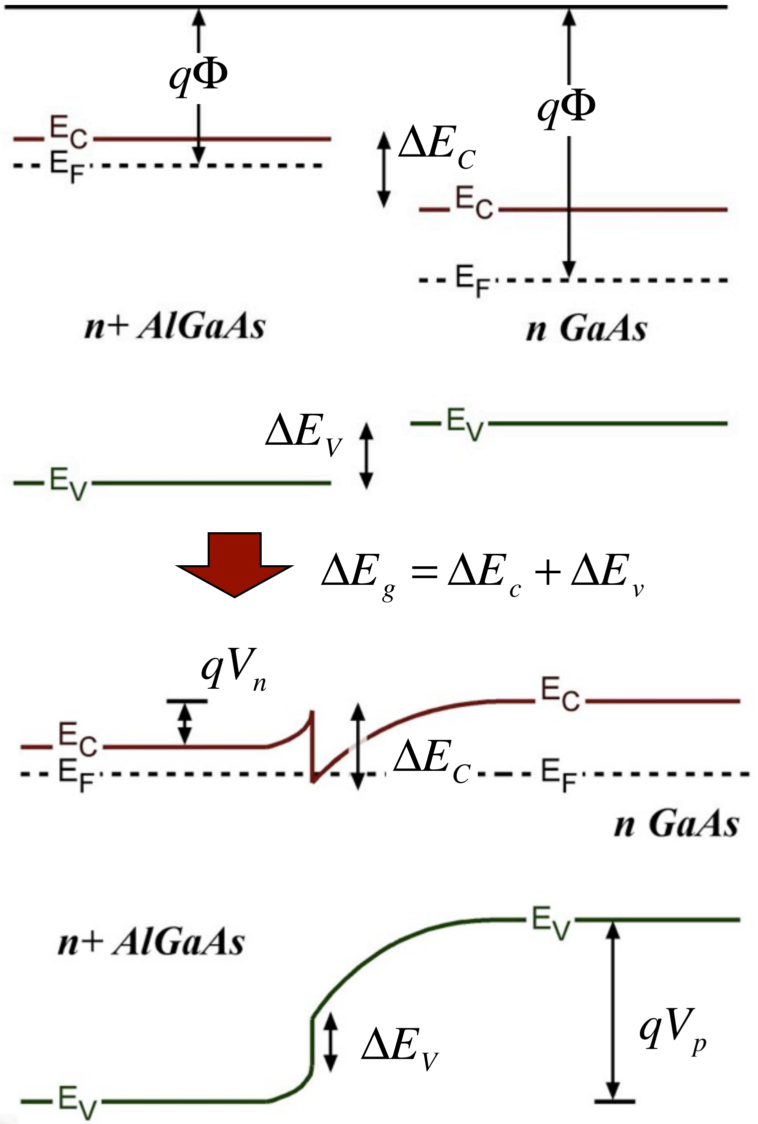
- Heterojunctions… joining two different semiconductors!

(1) Align Fermi levels (always!)

(2) Maintain ΔE_C and ΔE_V at the metallurgic (material) junction

(3) Connect E_c/E_v keeping E_g constant as bend bands, and as you do that…

(4) Consider doping effects to distribute the amount of band-bending due to $\Delta\Phi$



- Remember, electrons always settle in lower parts of the conduction band

- However, this is a very narrow well for holding electrons…

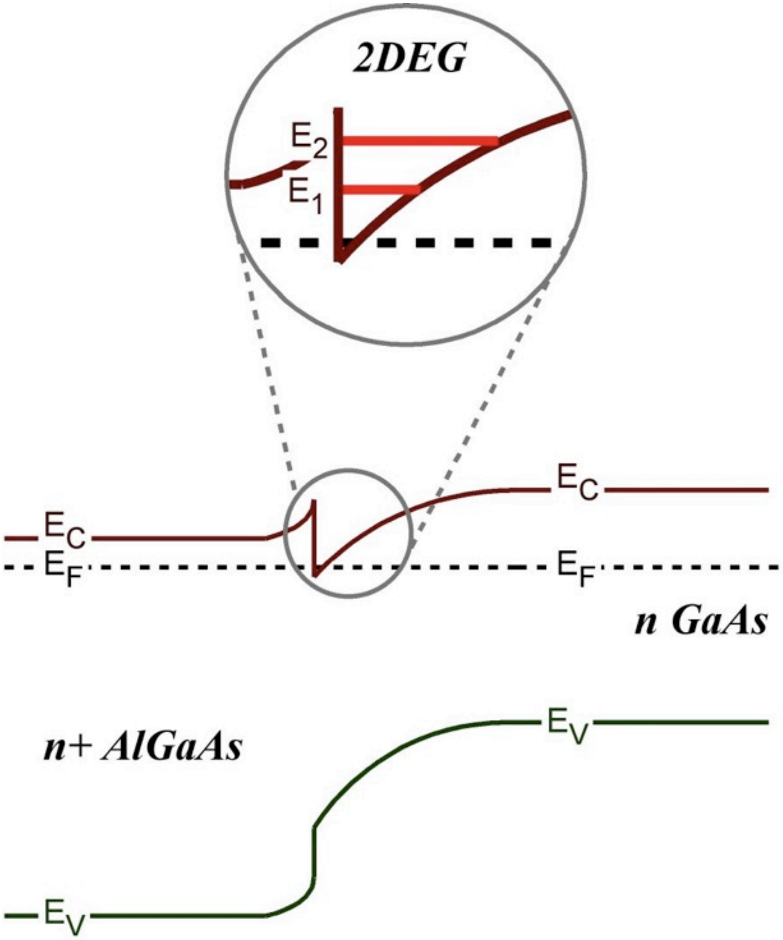
- *Quantum Well, Discrete E_n*

- Less scattering for the 2DEG so mobilities become huge!

10,000's! to 100,000's! Si typically < 1000!

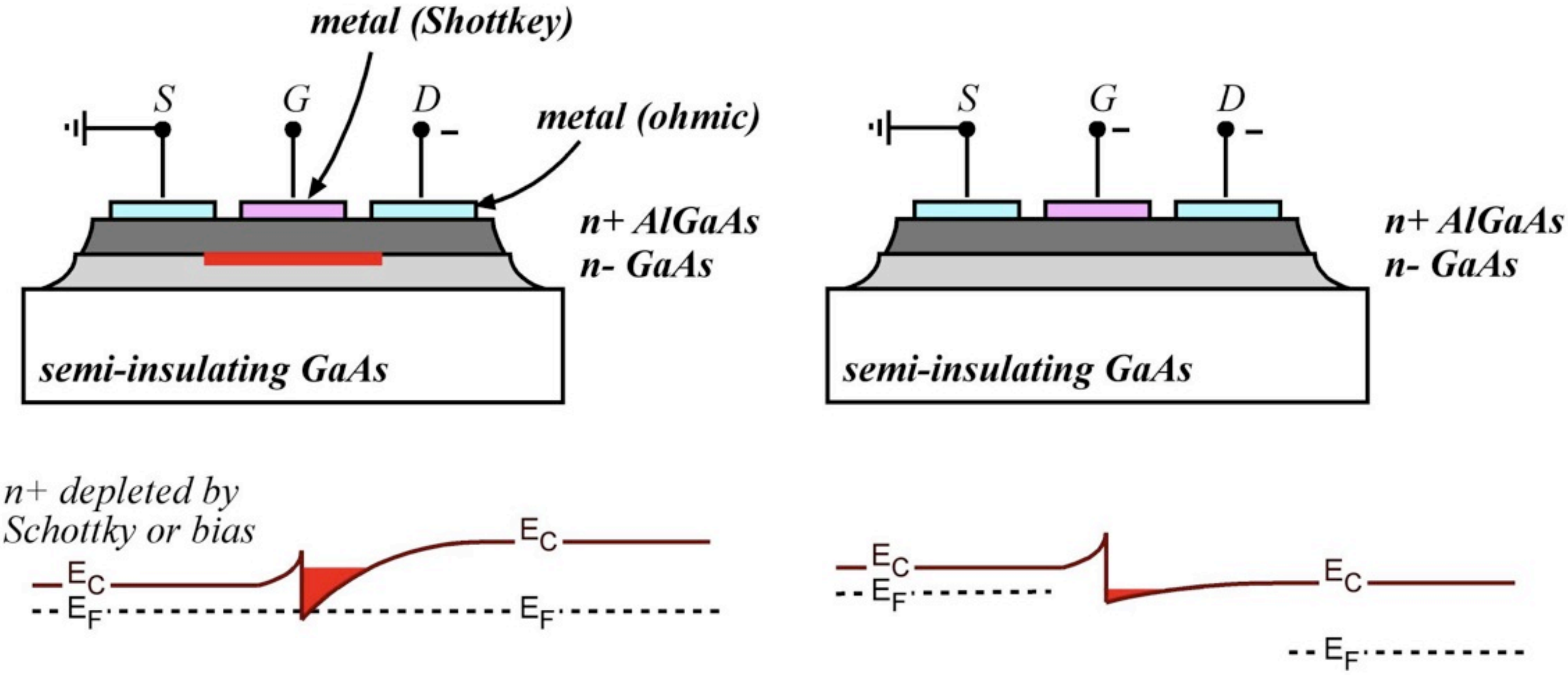
- **High Electron Mobility Transistor (HEMT)**

- Extremely fast speeds!
  (because of higher J)



Back to Heterojunctions…

- Depending on Schottky contacts, thickness of AlGaAs layer, and bias, device can be normally ON or OFF. Layers below the channel MUST be lightly doped!



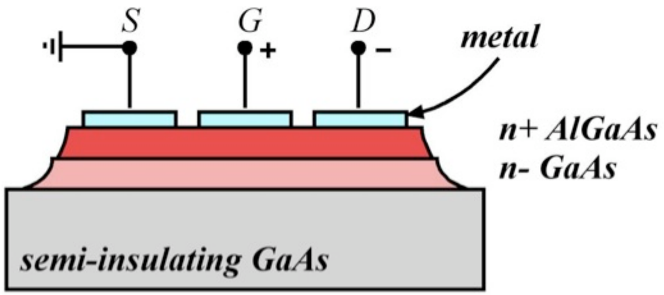
May need a Shottky gate to deplete the AlGaAs layer too (so no current from metal into n-GaAs layer, or through the AlGaAs itself).

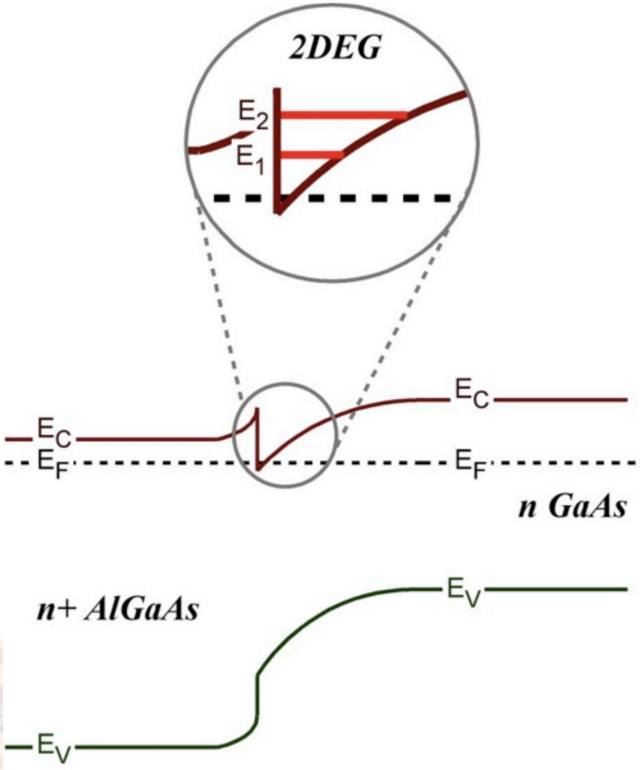
HEMT

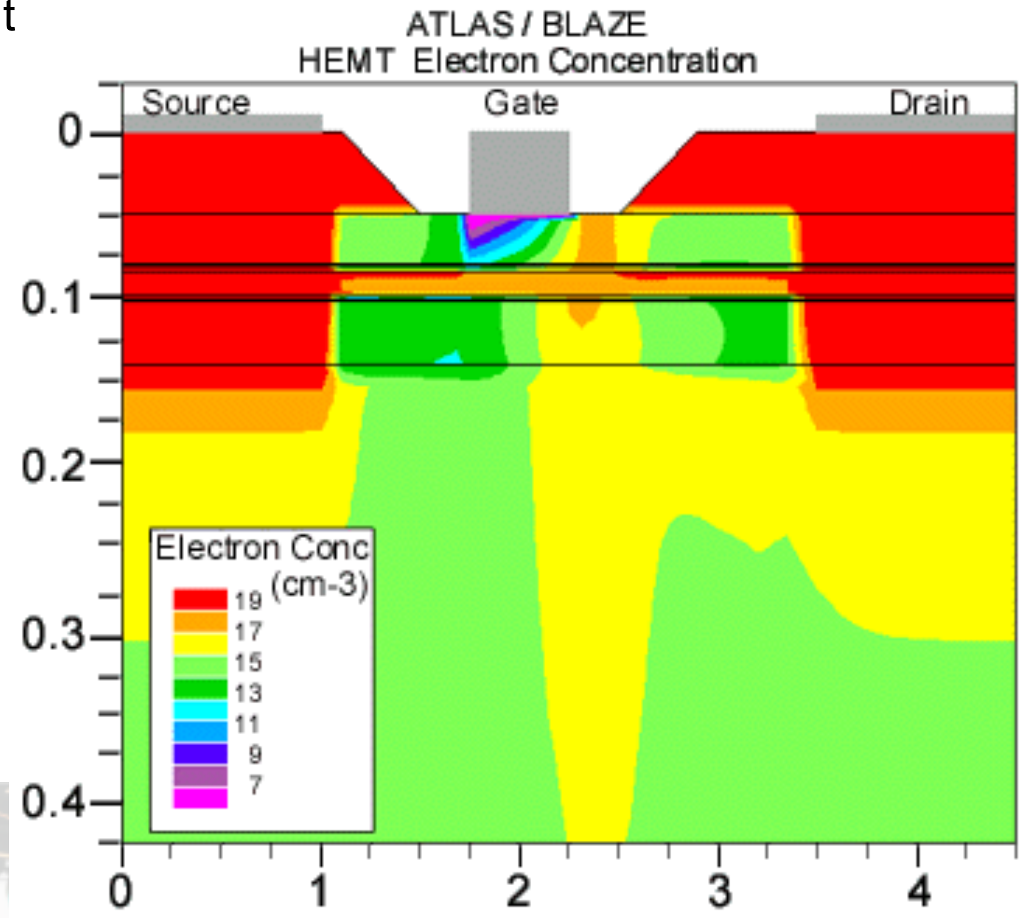
- Back to the picture of the day, without worrying too much about all the device details, where is the 2DEG?

- Is this device ON or OFF?

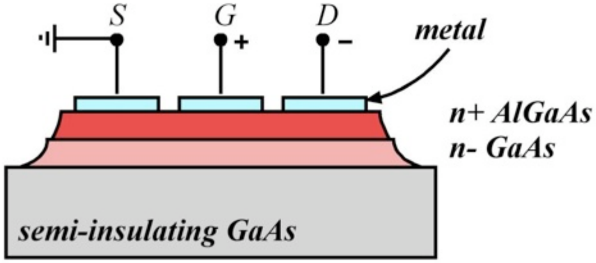
- See the depletion region, why is it triangular in shape?







HEMT



Other materials:
GaN
InP
InAs
etc… >500 GHz!

Oki Electric Develops GaN-HEMT on Silicon Substrate with Record High Amplifying Characteristics

Los Angeles, Calif. October 16, 2005 -- Oki Electric Industry Co., Ltd. (TSE: 6703) today announced the development of a power transistor with dramatically improved amplifying characteristics. This Gallium Nitride High Electron Mobility Transistor (GaN-HEMT), is formed on a large diameter silicon substrate achieving a world record for transconductance rating of **350mS/mm** and maximum oscillation frequency (fmax)(*1) of **115GHz.** Because this GaN-HEMT is achieved on a silicon wafer --not on conventional SiC (Silicon Carbide)--, it can reduce costs by approximately 50%. This will help wireless communication systems become lower power consumption, smaller and lower cost.

F.O.M.: 350mS/mm -> S=A/V, mm = width of device

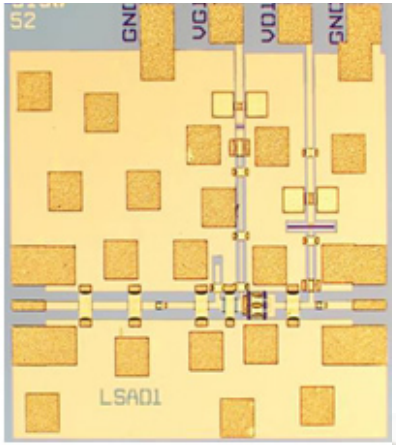


Figure 3. InP HEMT MMIC active doubler that demonstrated 100 microwatts of output power at 300 GHz.

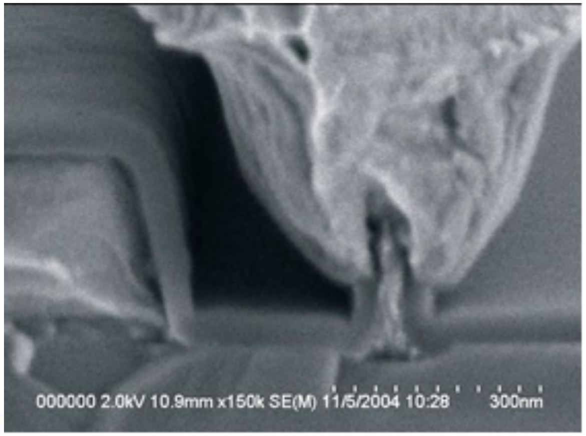


Figure 4. Scanning electron micrograph of a HEMT T-gate structure showing a metal gate footprint of approximately 50 nanometers encapsulated in dielectric material. Similar structures can be used for various quantum and spin-based devices.

HEMT

CREE

CGH40006P

6 W, RF Power GaN HEMT

Cree's CGH40006P is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40006P, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40006P ideal for linear and compressed amplifier circuits. The transistor is available in a solder-down, pill package.

Package Types: 440109
PN's: CGH40006P

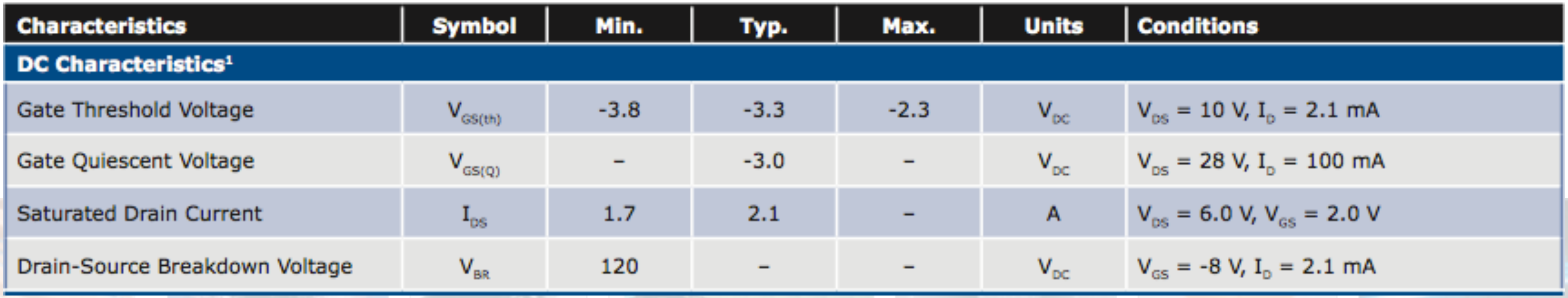
FEATURES

- Up to 6 GHz Operation
- 13 dB Small Signal Gain at 2.0 GHz
- 11 dB Small Signal Gain at 6.0 GHz
- 8 W typical at P_{IN} = 32 dBm
- 65 % Efficiency at P_{IN} = 32 dBm
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA

- This product is $48.96 from Digikey. 220 W (yes 220W) version is $896 at Digikey! (2011 pricing)



Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.3	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 2.1 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-3.0	–	V_{DC}	V_{DS} = 28 V, I_D = 100 mA
Saturated Drain Current	I_{DS}	1.7	2.1	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 2.1 mA

So many transistor types!

- Lastly, how to tell different transistors apart… (but you will find not everyone follows this!).

Why the arrow directions at JFET gates?

- After next week, you will also understand why MOSFETs look the way they do…

	JFET-N Transistor	N-channel field effect transistor
	JFET-P Transistor	P-channel field effect transistor
	NMOS Transistor	N-channel MOSFET transistor
	PMOS Transistor	P-channel MOSFET transistor
	NPN Bipolar Transistor	Allows current flow when high potential at base (middle)
	PNP Bipolar Transistor	Allows current flow when low potential at base (middle)

Review! Take a Break!

- Why do people create and use MESFETs? *There are three advantages we highlighted…*

- What kind of equations are needed to predict JFET and MESFET performance? *Hint, this whole course is dominantly built on one type of two-terminal semiconductor device and its equations!*

- Why do people create and use HEMTs? *There is one big reason why…*

- How much bigger is the channel mobility for a GaAs HEMT vs. GaAs MESFET? vs. a Si JFET?

Look up a few mobilities from the slides, to get an appreciation for how they compare in channel mobility (which leads to channel conductivity).